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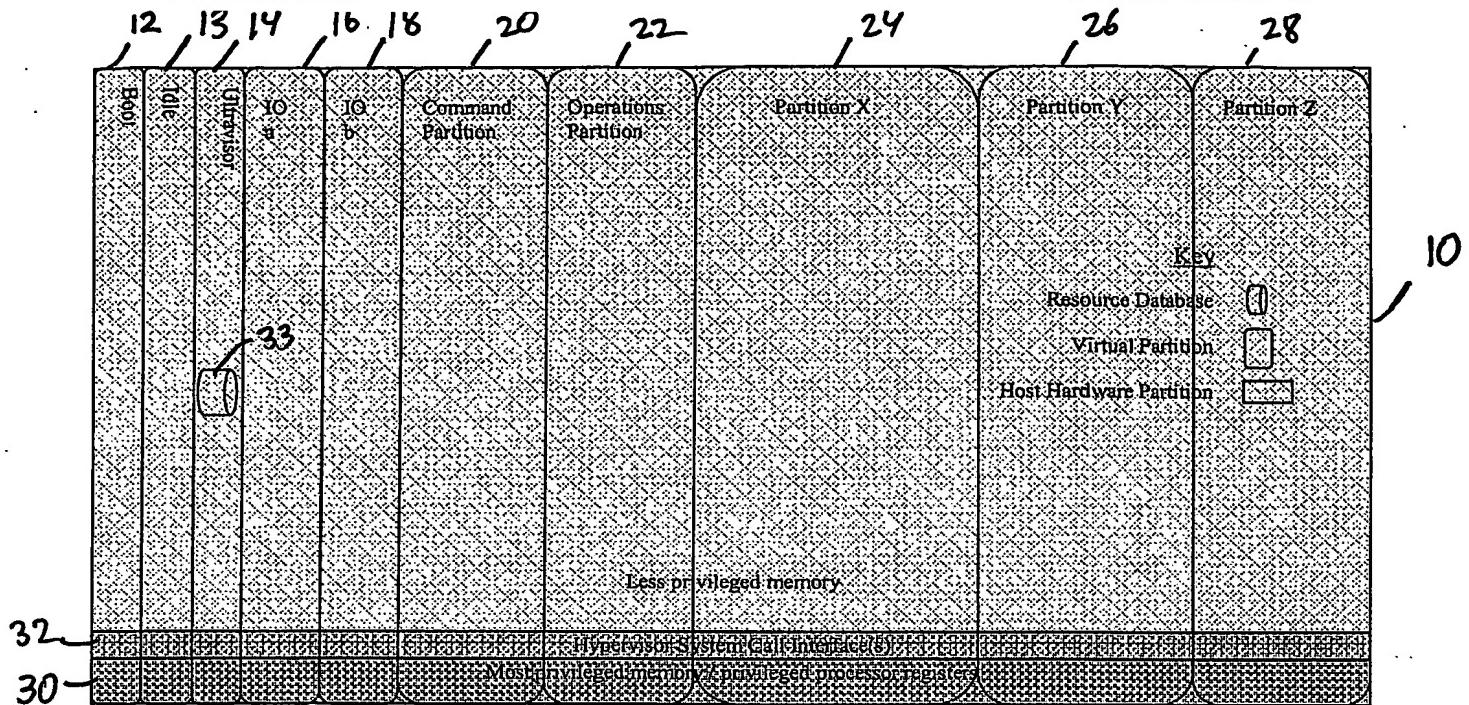


Figure 1: Partitioned Host System

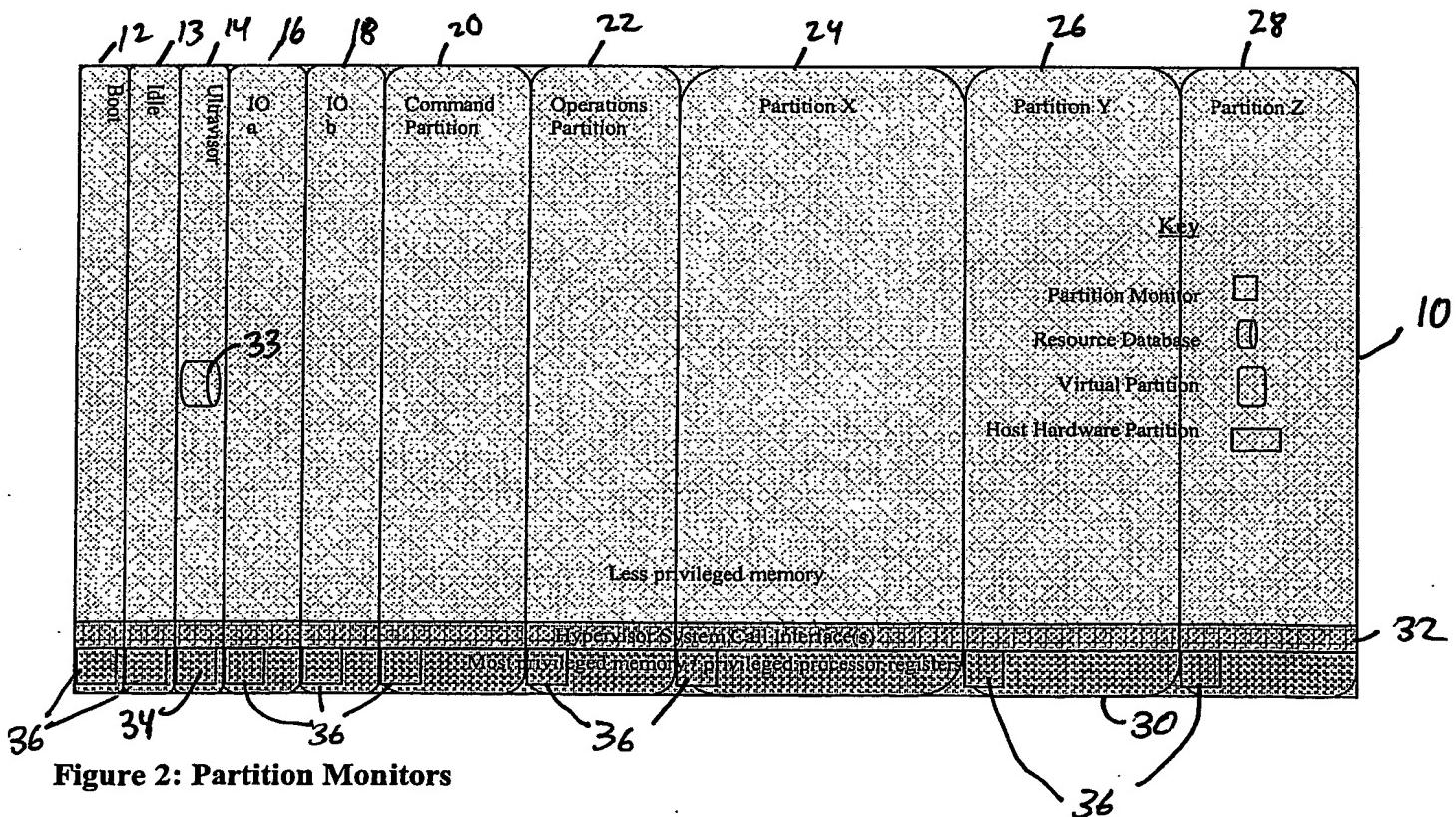


Figure 2: Partition Monitors

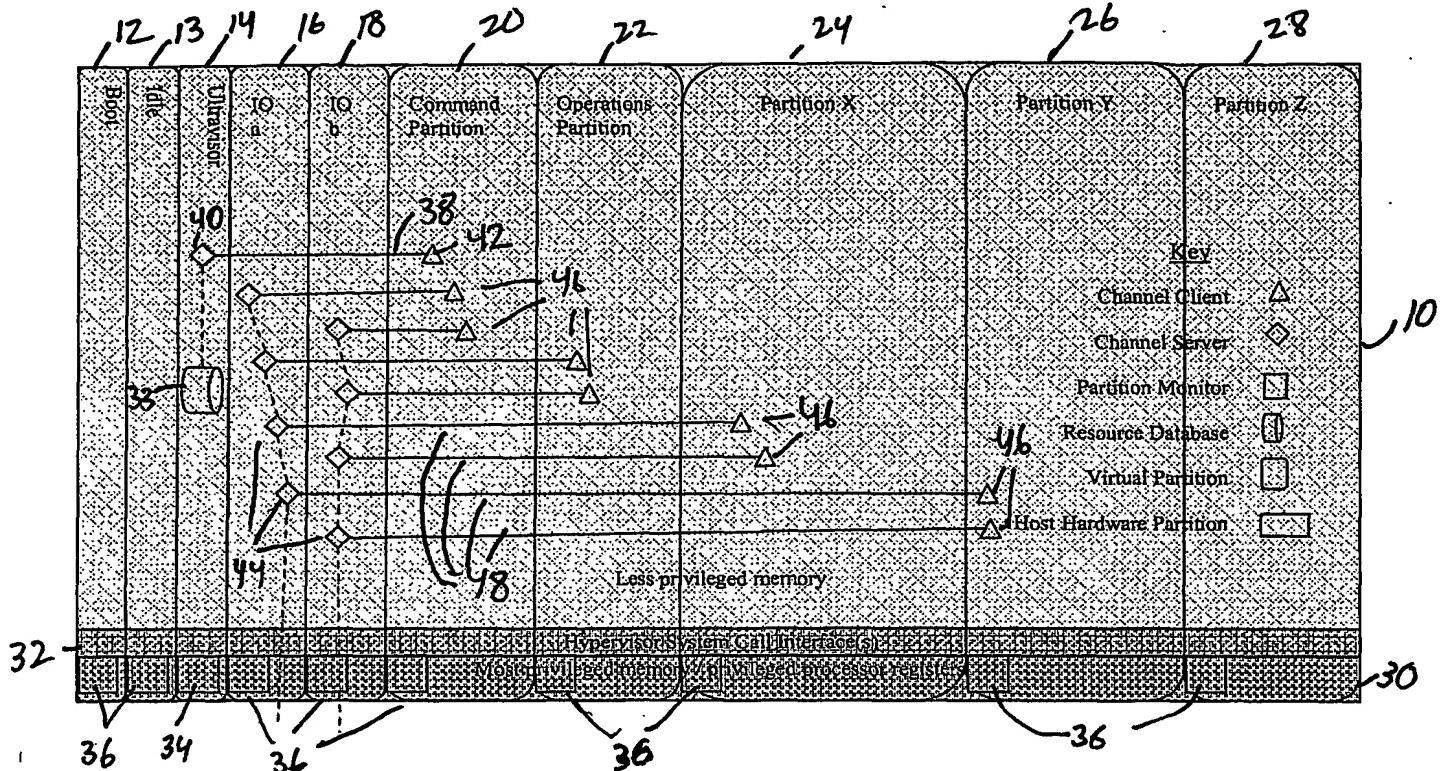


Figure 3: Partition Channels

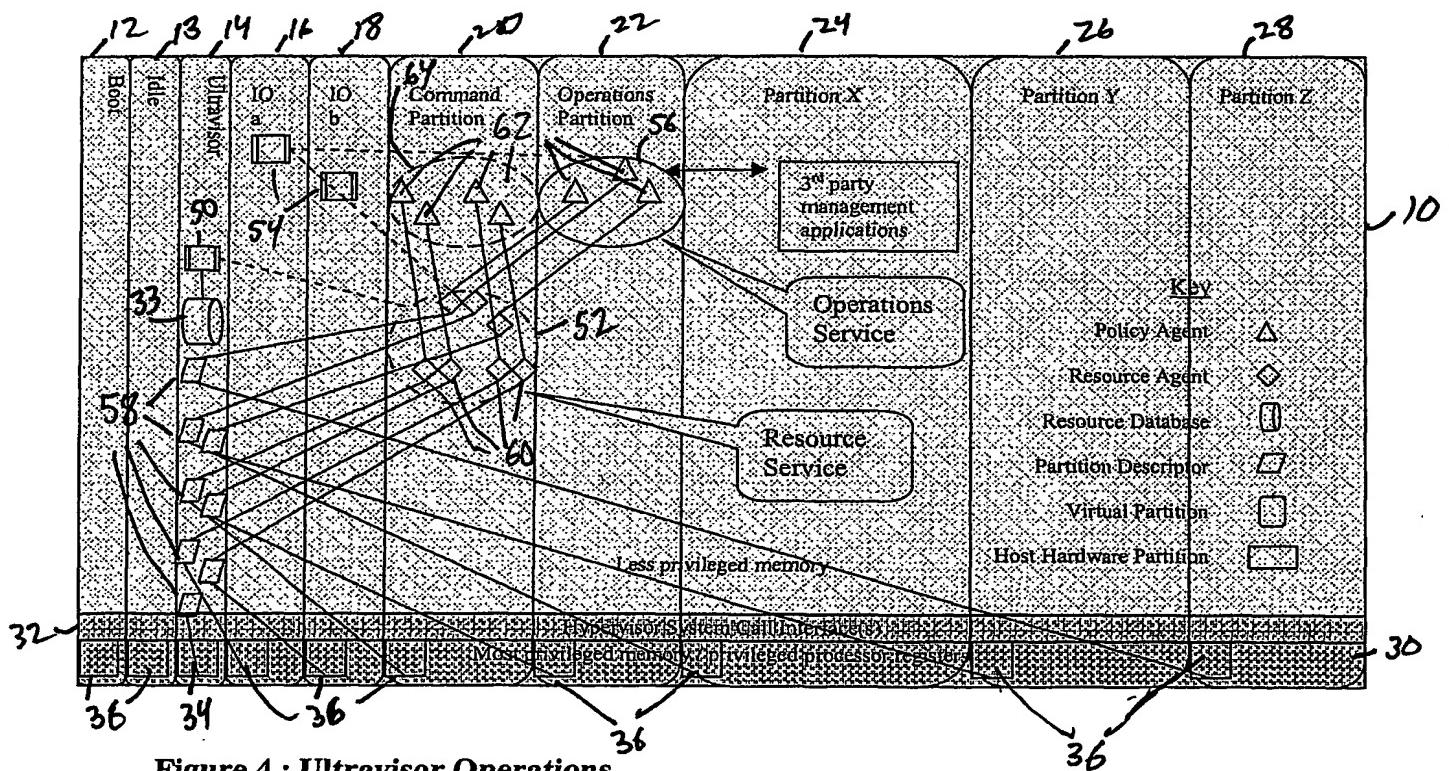


Figure 4 : Ultrvisor Operations

Overlapped processor throttling – default 4 bit duty width (1/16 = 6.25%)

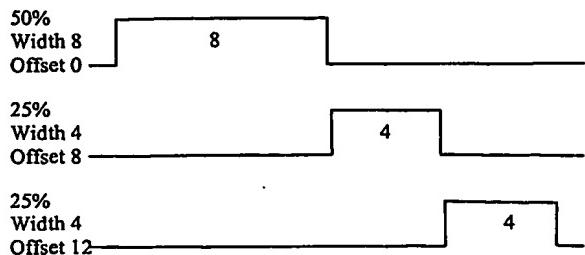


Figure 5 : Processor Sharing

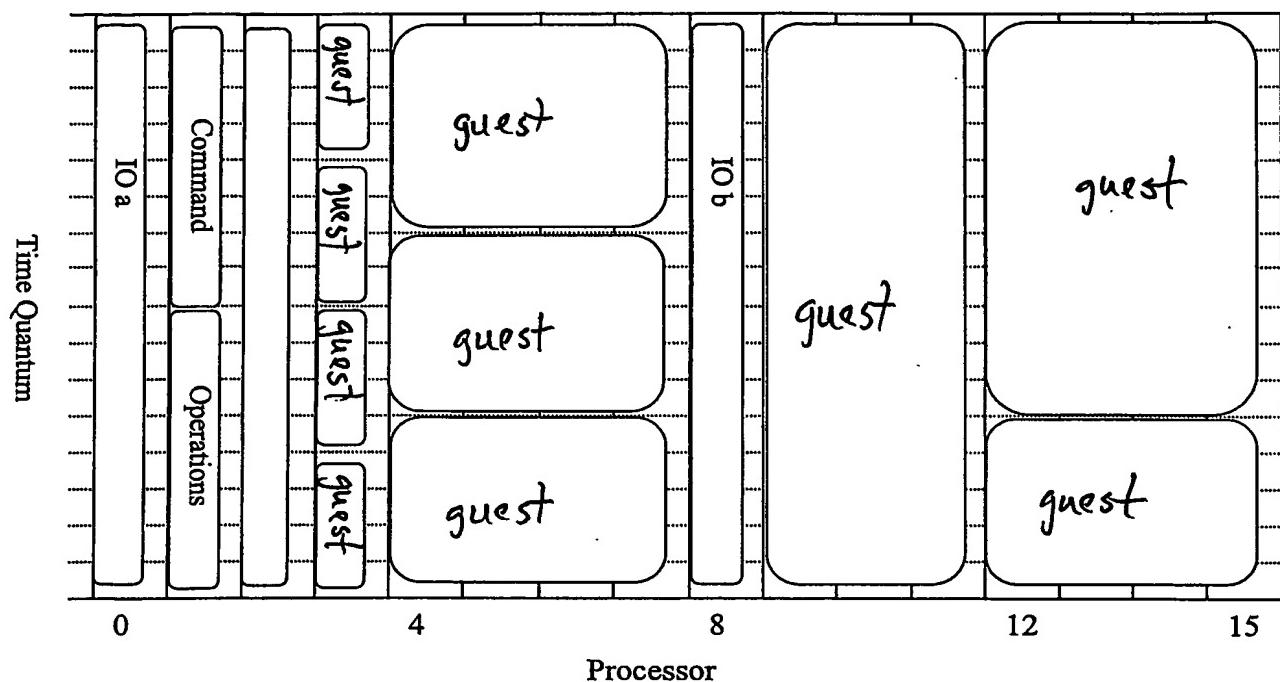


Figure 6 : Processor Schedule

$(2^{10})^n$	SI prefix	SI name	Page Table	Pageantry	IA32/EM32T
1	K	kilo	PKM	PKE	PT/PTE
2	M	mega	PMM	PME	PD/PDE
3	G	giga	PGM	PGE	PDP
4	T	tera	PTM	PTE	PML4
5	P	peta	PPM	PPE	
6	E	Exa	PEM	PEE	
7	Z	zetta	PZM	PZE	
8	Y	yotta	PYM	PYE	

Figure 7 : SI Prefixes for Page Table Hierarchy

Function GetMemoryOwner [T : 0..1023, G:0..1023, M:0..1023, K:0..1023] of Int32

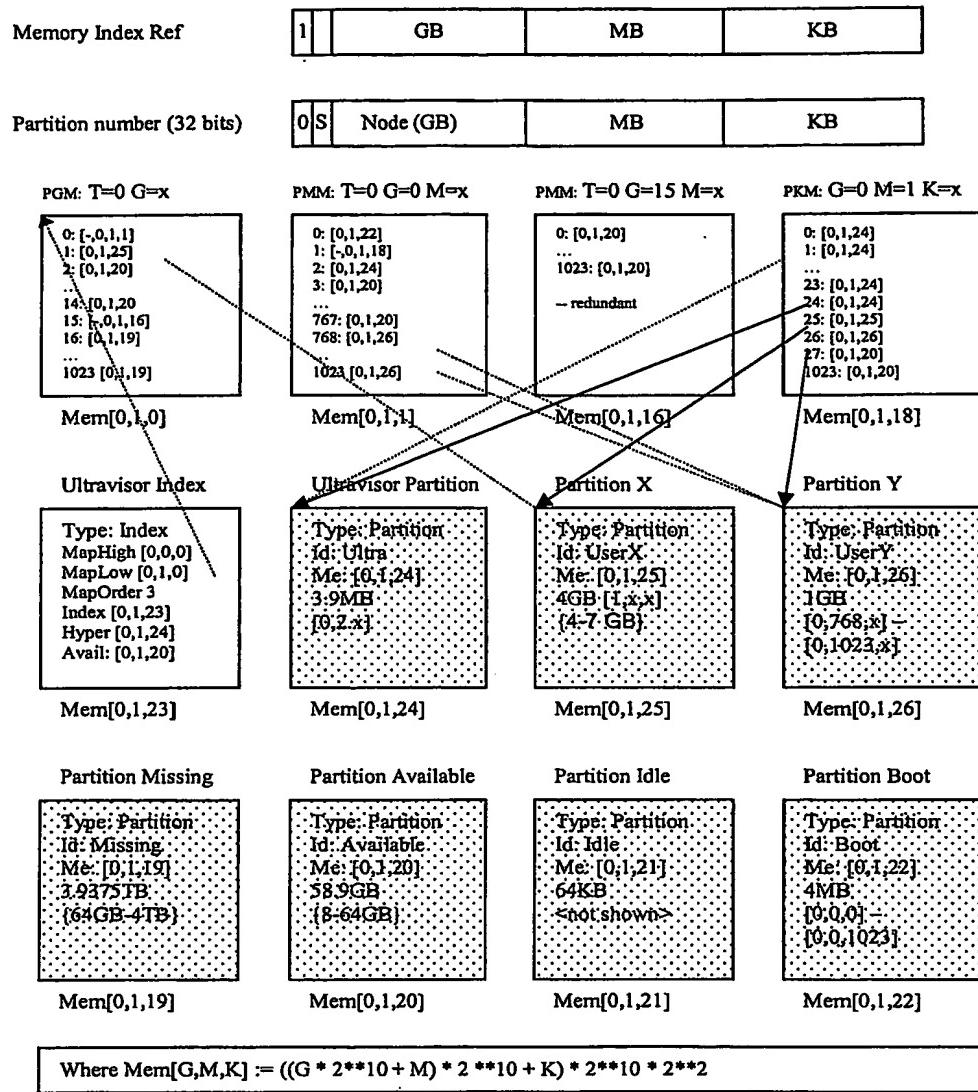
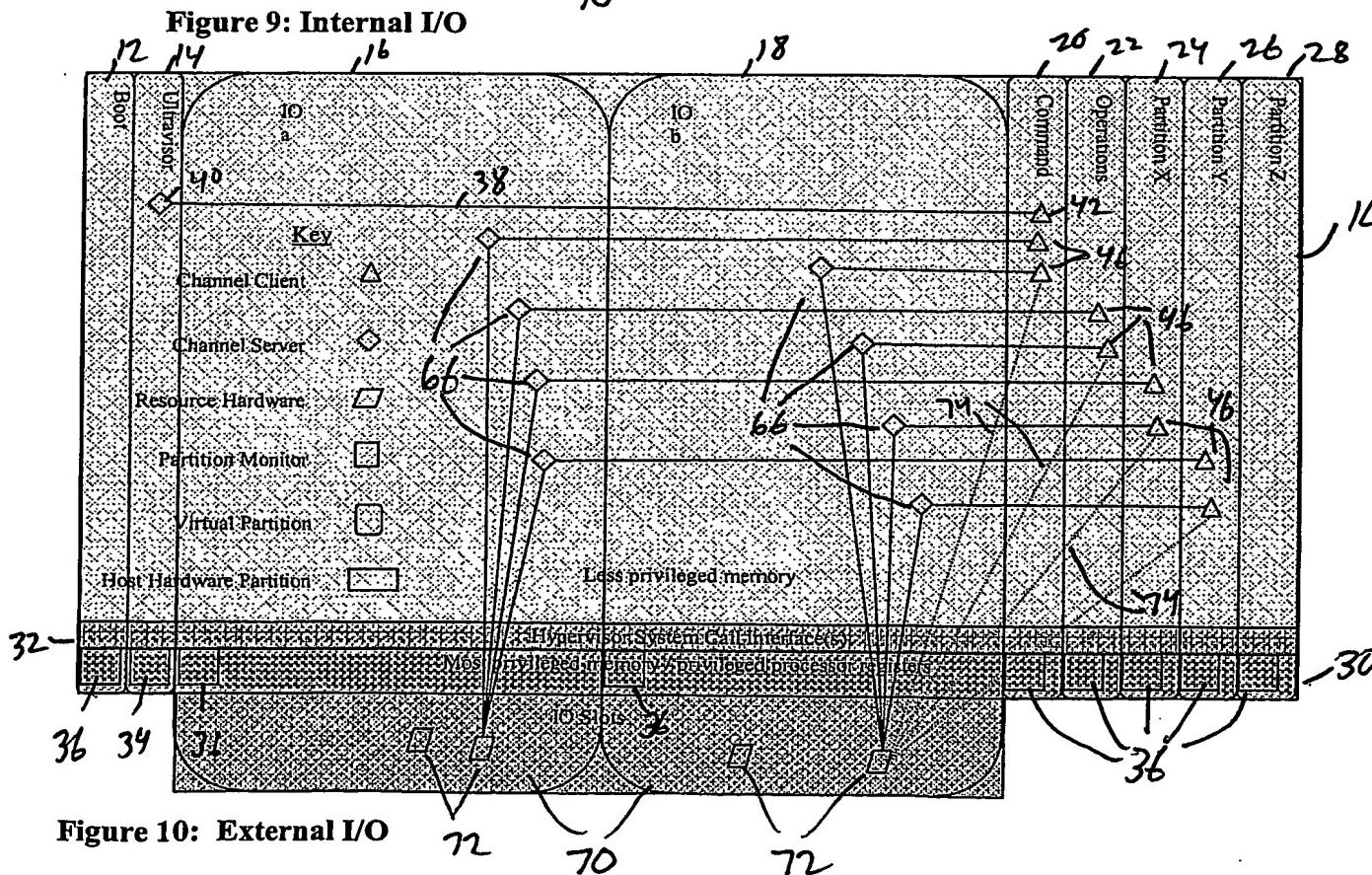
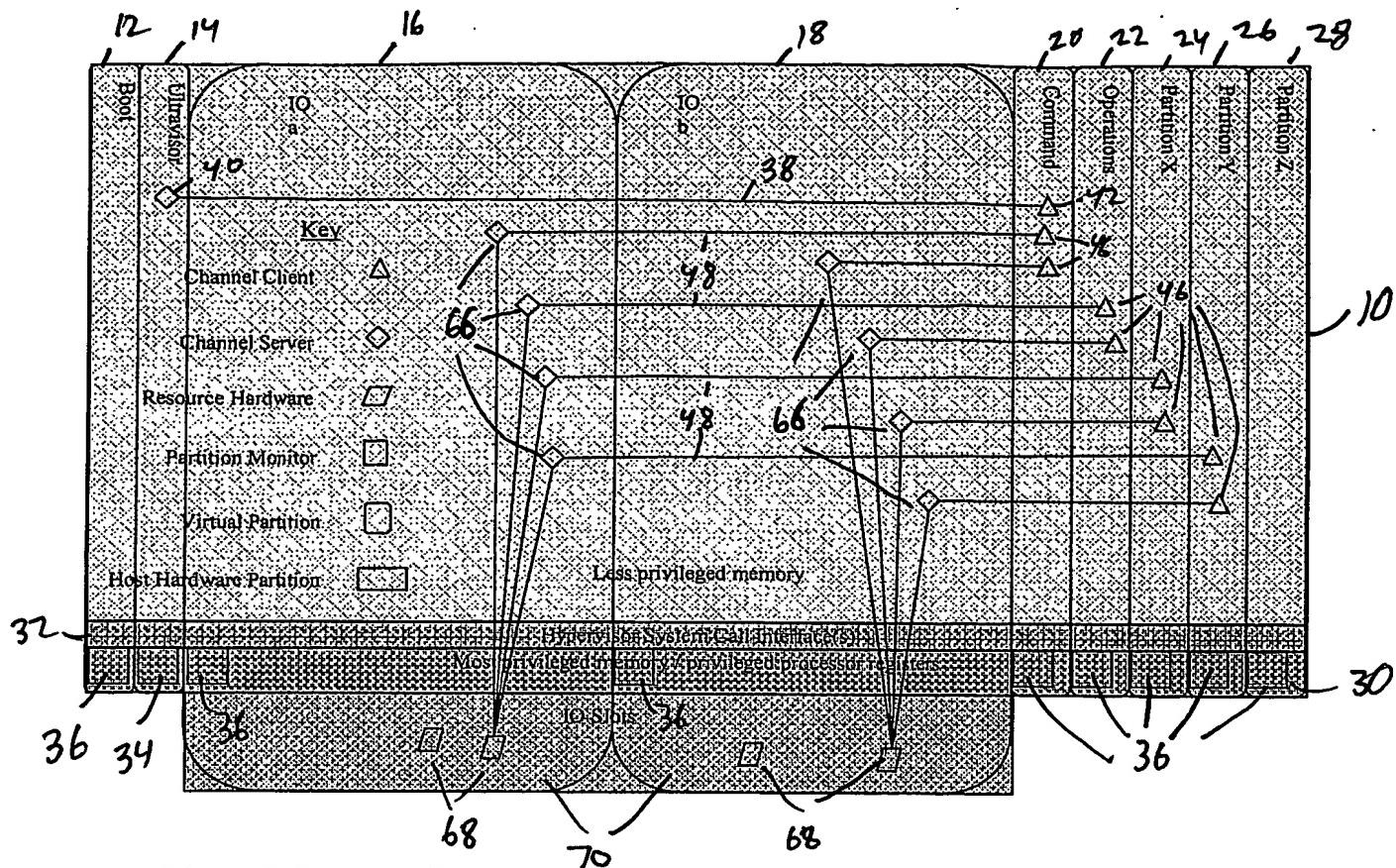
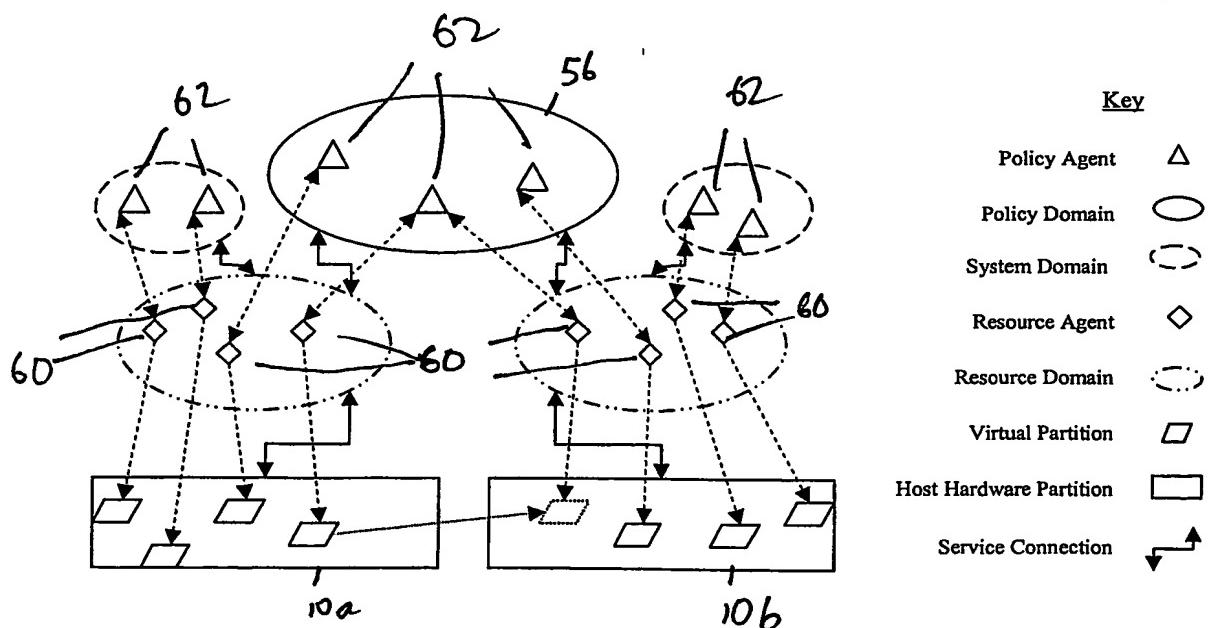
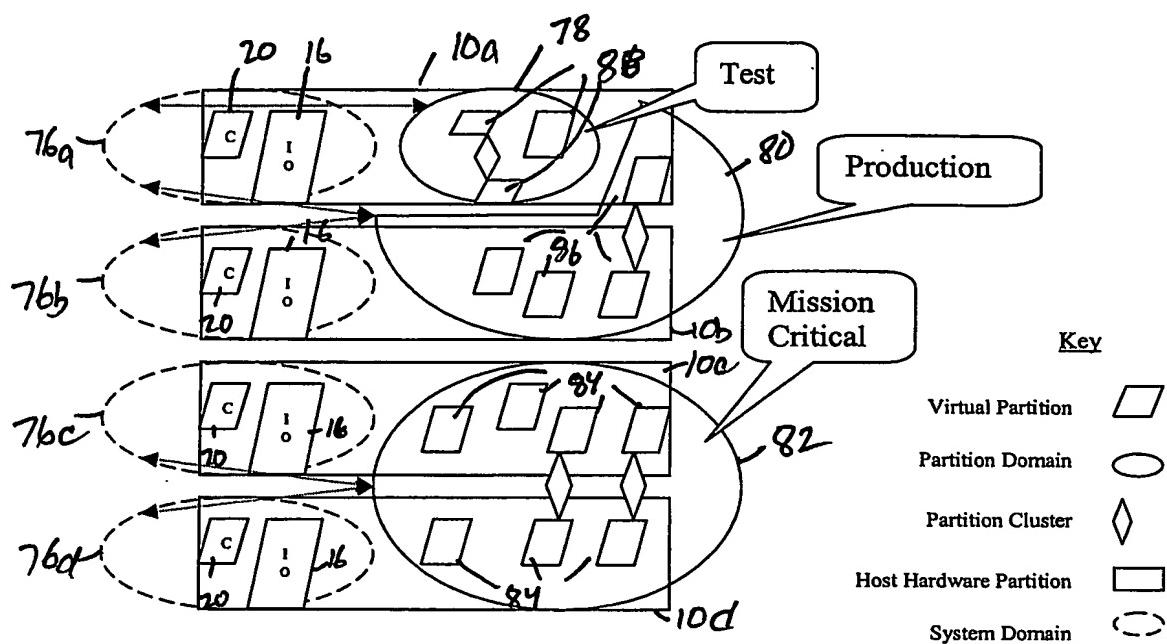


Figure 8 : Partition Memory Map





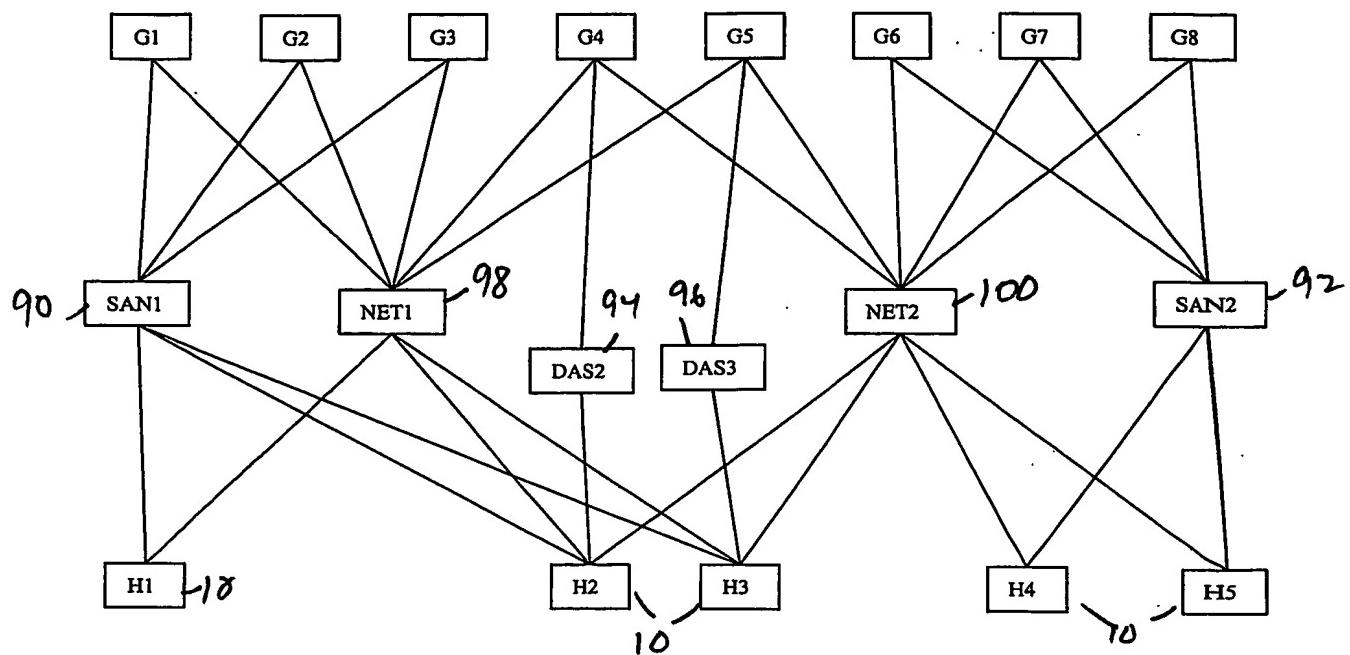


Figure 13 : Virtual Data Center Zones

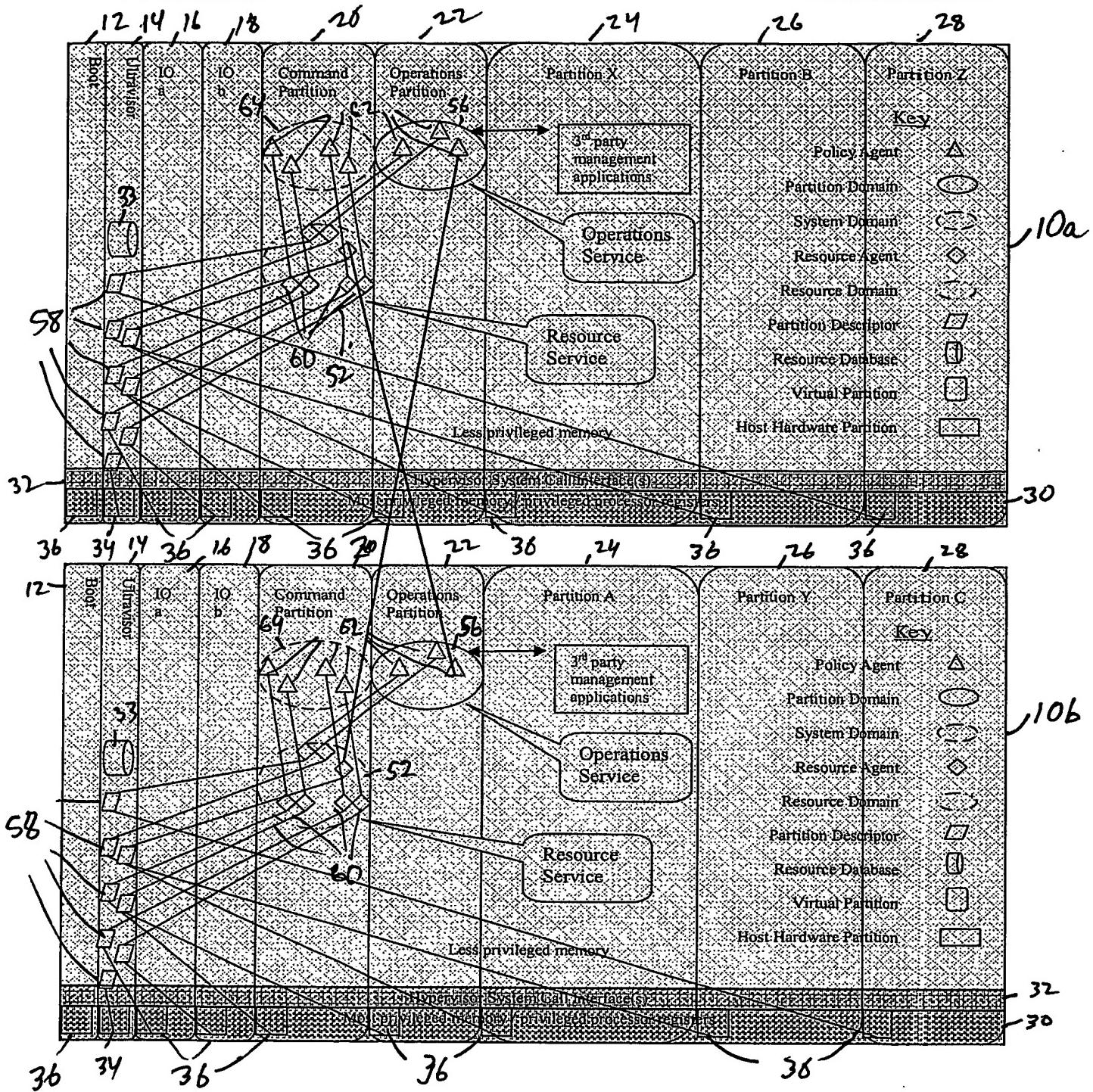


Figure 14 : Data Center/Multiple Hosts

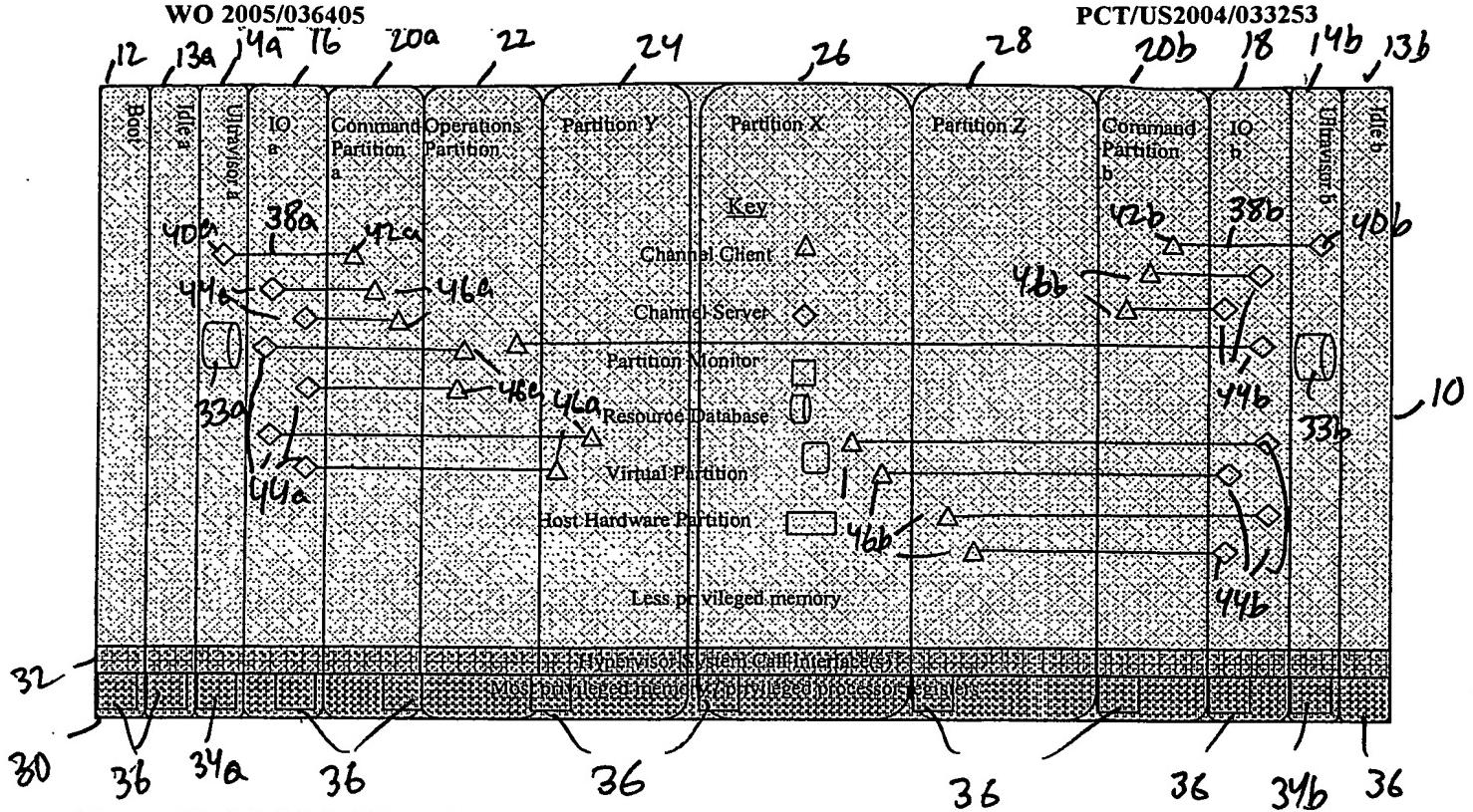


Figure 15: Multiple Ultravisor Resource Partitions

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